The Design of a CMOS Nanoelectrode Array With 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/Stimulation of Mammalian Neurons

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Abstract—CMOS microelectrode arrays (MEAs) can record electrophysiological activities of a large number of neurons in parallel but only extracellularly with a low signal-to-noise ratio. Patch-clamp electrodes can perform intracellular recording with a high signal-to-noise ratio but only from a few neurons in parallel. Recently, we have developed and reported a neuro-electronic interface that combines the parallelism of the CMOS MEA and the intracellular sensitivity of the patch clamp. Here, we report the design and characterization of the CMOS integrated circuit (IC), a critical component of the neuro-electronic interface. Fabricated in 0.18-µm technology, the IC features an array of 4096 platinum black (PtB) nanoelectrodes spaced at a 20-µm pitch on its surface and contains 4096 active pixel circuits. Each active pixel circuit, consisting of a new switched-capacitor current injector—capable of injecting from ±15 pA to ±0.7 µA with a 5-pA resolution—and an operational amplifier, is highly configurable. When configured into the current-clamp mode, the pixel intracellularly records membrane potentials, including subthreshold activities with ~23-µV_{rms} input-referred noise while injecting a current for simultaneous stimulation. When configured into the voltage-clamp mode, the pixel becomes a switched-capacitor transimpedance amplifier with ~1-pA_{rms} input-referred noise and intracellularly records ion channel currents while applying a voltage for simultaneous stimulation. Such voltage-/current-clamp intracellular recording/stimulation is a feat only previously possible with the patch-clamp method. At the same time, as an array, the IC overcomes the lack of parallelism of the patch-clamp method, measuring thousands of mammalian neurons in parallel, with full-frame intracellular recording/stimulation at 9.4 kHz.

Index Terms—Current clamp, extracellular recording, integrated circuits (ICs), intracellular recording, microelectrode array (MEA), nanobiointerface, nanoelectrode array, neurobiology, neurons, switched capacitor, voltage clamp.

I. INTRODUCTION

CMOS microelectrode arrays (MEAs) have served as an important tool in neurobiology with their ability to record membrane potentials from a large number of neurons, with the state-of-the-art featuring as many as 10 000’s of recording channels [1]–[14]. However, this neuronal recording by the CMOS MEA is an extracellular technique. The voltage it records outside the neuron is a highly attenuated and filtered version of the actual membrane potential inside the neuron, e.g., action potentials (APs) with intracellular amplitudes of ~100 mV are attenuated to below ~100 µV at the extracellular electrode, and their intracellular duration of ~10 ms is reduced to as short as 100 µs at the extracellular electrode [12]. Given such a large attenuation through the extracellular neuron–microelectrode interface, the CMOS MEA cannot record small but critical synaptic events, such as postsynaptic potentials (PSPs), whose intracellular amplitudes are less than ~5 mV. Another related drawback of the CMOS MEA is the inability for concurrent stimulation and recording of a neuron through the same electrode, as an extracellular stimulation signal needed is over 10³× larger than the extracellularly recorded signal [15].

In contrast, the patch-clamp technique, the gold standard of high-fidelity electrophysiological recording, directly accesses
the intracellular solution of a neuron with no attenuation by mechanically puncturing its membrane followed by a tight-sealing [16]. The resulting intracellular recording has a far higher sensitivity than the CMOS MEA and can routinely measure synaptic activities. This intracellular recording can be also simultaneously performed with stimulation in the form of current clamp (membrane potential recording with current injected) or voltage clamp (membrane current recording with the voltage applied). The current- and voltage-clamp modes are used for a variety of electrophysiological interrogation of neurons. For example, the current clamp recording of PSPs can find synapses, and the voltage clamp, which was used for the first measurement of currents of single ion-channel molecules [17], can characterize the effect of drugs on ion channels. This highly sensitive patch-clamp electrode, however, cannot be scaled into a dense array, such as the CMOS MEA, and only ~10 parallel patch neuron recordings have been possible so far [18].

Recently, nanoelectrode and microelectrode of the 3-D structure were studied for the possibility of intracellular access [19]–[20]. Some of them are also scalable, defined by top–down fabrication, and so have been hoped for combining the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA. However, only a few of them [22], [23], [26], [27] could couple intracellularly with mammalian neurons and even then, only on a single or few neuron basis, and without the current-/voltage-clamp configurations, thus lacking the capability for simultaneous recording and stimulation through the same electrode.

We have very recently developed a scalable, $64 \times 64 = 4096$ platinum black (PtB) nanoelectrode array on a CMOS integrated circuit (IC), which bridges the previous gap between the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA and performs massively parallel intracellular recording from thousands of connected mammalian neurons [31]. The CMOS IC realizes current-/voltage-clamp electronics for each of the 4096 sites or pixels. At an individual pixel, both the surface PtB nanoelectrode interfacing with a neuron and the underlying CMOS voltage/current clamp electronics operating the PtB nanoelectrode are critical for the stable intracellular recording/stimulation of the neuron. At the same time, its arrayed operation gives rise to the parallelism.

In [31], we reported network-wide intracellular recording with this chip and its application in synaptic connectivity mapping and high-throughput drug screening. This article complements [31], reporting the design of the CMOS IC, describing, in detail, how it enables the intracellular neuronal recording with simultaneous stimulation using current/voltage clamp, a feat only previously possible with the patch-clamp technique, and how it parallelizes such high-fidelity recording across the array, overcoming the limitation of the patch clamp.

Section II overviews the CMOS IC. Section III presents the pixel circuit and its current- and voltage-clamp configurations. Section IV presents the new, switched-capacitor-based current injector, a crucial pixel circuit component. Sections V and VI present electrical and electrophysiological characterizations.
array for high spatial resolution and the large $100 \times 250-\mu m^2$ area for each active pixel circuit for high configurability and low noise. This layout strategy combines the concepts of high-fidelity peripheral electronics from the switched matrix CMOS MEAs [3], [8], [11], [13] and the full-frame readout of the active-pixel sensor (APS) CMOS MEAs [1], [2], [7], [14].

The metallic routing from a pixel circuit to its electrode has a length of $\sim 1 \sim 10$ mm, depending on the location of the pixel circuit and its electrode. To mitigate the capacitive coupling between adjacent routings, we surround each routing with ground shields (Fig. 2, left). This reduces the cross-coupling capacitance to $<1$ fF per routing, virtually ensuring no cross-contamination between different electrode signals (see Section V-D). We minimize the parasitic capacitance $C_{p,r}$ between an individual routing and its shield by gradually increasing the spacing between them, as the density of the routings decreases further away from the electrode array. $C_{p,r}$ is $\sim 1\text{–}2$ pF in electric field simulations (Fig. 2, right for the densest routings). The routings and shields use four of the available six metal layers and occupy $\sim 1.5 \times 20$ mm$^2$ in total.

To enable accurate temperature regulation, the IC contains two temperature sensors (based on the voltage differential between two diode branches of different sizes, 1:146 ratio, biased at the same current) and a heater (a 10-Ω poly-silicon resistor capable of dissipating 1.3 W) adjacent to the electrode array (see Fig. 1(a)). They regulate the temperature of the IC to $34 \text{°C} \sim 37 \text{°C}$ for cell health (see Section V-A).

The design of this IC with the particular choice of the architecture, building blocks, and target performance is guided by our goal to demonstrate the unprecedented massive parallelism in the intracellular recording of neurons. For example, we focus our design efforts significantly on realizing the front-end current/voltage-clamp capability in each active pixel circuit, as it is essential for robust intracellular access into neurons; on the other hand, for the back-end digitization that is not fundamental to the key demonstration goal, we choose to use commercially-available high-precision analog-to-digital converters (ADCs) in order to accelerate the chip development. To drive such off-chip electronics, we implement high-speed analog multiplexers on chip. They require large bias currents to operate at frequencies in excess of 1 MHz, but, in our

in vitro setting, the associated heat readily sinks through the open well of the solution on the chip. In fact, we actually need explicit heating of the solution to keep the cells at the temperature around $35 \text{°C}$. This is in contrast to implantable applications [32], where an IC insulated by biological tissue should maintain low power density to prevent tissue damage.

III. Active Pixel Circuit

Fig. 3(a) shows the schematic of the active pixel circuit. Its main components are a switched-capacitor current injector (see Section IV) and an op-amp with configurable negative feedback networks, both of which are connected to the same PtB electrode of the pixel. It also contains a transparent latch digital memory and an output multiplexer (shared by 128 pixels per multiplexed analog output). The pixel circuit contains many transmission gate switches, controlled by the digital memory programmable in real time at up to $\sim 10$ MHz. Many of these switches are in the op-amp negative feedback networks, making the closed-loop amplifier highly configurable. Four voltage nodes, $V_{s,i} \sim V_{s,r}$, can be connected to various voltage signals or bias references from off-chip electronics, supporting the high configurability as well as various tests. Of the pixel circuit area of $0.025 \text{ mm}^2$ [see Fig. 3(b)], the op-amp takes the largest part due to large transistors (see Section IV). A dedicated bias network is included for each pixel, as opposed to a global bias, in order to help isolate the 4096 op-amps. The current injector occupies only $\sim 0.003 \text{ mm}^2$, almost an order of magnitude smaller than standard current injectors used in MEAs [6], [9], [11], [13], attesting to the advance of our novel design (see Section IV).

For intracellular recording/stimulation, we operate the pixel circuit of Fig. 3(a) in pseudo-current- or pseudo-voltage-clamp mode (see Fig. 4), named after the similar configurations of the patch clamp. “Pseudo” emphasizes that our intracellular interface has a finite attenuation, unlike the patch clamp, as shown in the following.

A. Pseudo-Current-Clamp (pCC) Configuration

The pCC mode [see Fig. 4(a)] is obtained from Fig. 3(a) by operating the high output impedance current injector in parallel with the op-amp with the negative feedback configured as a high input impedance voltage amplifier. The current injector runs a current $I_e$ through the electrode. This continuously injected $I_e$ (typically on the order of $\sim 1$ nA) causes and sustains the membrane permeabilization in a neuron to initiate and maintain intracellular coupling [31]. Another crucial role of this current injection is to compensate for the leakage current from within the neuron that inevitably arises due to the membrane permeabilization. At the same time, the voltage amplifier concurrently measures the electrode voltage $V_e$, which is an attenuated version of the membrane potential $V_m$.

In this way, we intracellularly record membrane potentials (APs and PSPs) of the neuron. This operation is akin to the patch clamp’s current-clamp recording.

The voltage amplifier is a bandpass configuration, traditionally used for low-noise neural recordings [33] [see Fig. 4(a)]. Its passband gain from $V_e$ to the amplifier output $V_{\text{amp}}$ is
the ratio of the feedback capacitors \( C_1/C_2 \). This is tunable: \( C_1 \) is 3.5 pF, but \( C_2 \) can be any addition of \(~5, ~20, \) and \(~100\) fF [see Fig. 3(a)]. The amplifier bandwidth covers the electrophysiological spectral range: \(~1\) Hz–5 kHz [34]. The low-frequency pole, \( f_1 \sim 1\) Hz, is set by \( C_2 \) in parallel with the large resistance of feedback antiparallel diode pairs (dps) [options for 1–7 dps; Fig. 3(a)] biased near-zero current. The more the dps, the less the voltage drop on each dp, reducing the nonlinearity and increasing the resistance. These dps are realized using \( p \) contacts within an n-well and contain parasitic reversed biased \( p n \) diodes to the substrate and corresponding leakage currents. An additional dp tapped to \( V_e \), sets a small current to tune the dc level of \( V_{\text{amp}} \) to overcome these leakage currents and to fine-tune the feedback resistance, which we discuss experimentally in Section V-C. The high-frequency pole \( f_2 \) is set by the gain-bandwidth product of the amplifier.

In the pCC recording, a change of the membrane potential \( V_m \) modulates the electrode voltage \( V_e \) according to

\[
\frac{\Delta V_m}{\Delta V_e} \approx R_s \frac{R_m}{R_{jm} + R_m}
\]

where \( R_s \) is the seal resistance, \( R_m \) is the junctional membrane resistance, and \( Z_1, Z_{p,r}, \) and \( Z_e \) are the impedances of \( C_1, C_{p,r}, \) and the PtB electrode. The approximation in the last step of (1) is due to \(|Z_e| \ll \|(Z_{p,r}||Z_1)\|\), which holds as the surface roughness; thus, the large surface area of the PtB electrode greatly reduces \( Z_e \) (see Section V-D). The front-end attenuation of (1) precedes the amplifier gain, contrasting the patch clamp’s current clamp that has no such front-end attenuation (hence the prefix, “pseudo” in our current clamp). However, as seen shortly, this attenuation is far less than that of the extracellular recording.

For stimulation, we change \( I_e \) to modulate \( V_m \) according to

\[
\frac{\Delta V_m}{\Delta I_e} \approx R_s \frac{R_m}{R_{jm} + R_m}
\]

where \( R_m \) is the membrane resistance. Here, we have assumed \( R_s \ll R_{jm} + R_m \), which holds for most nanoelectrodes (typical values: \( R_s < 100 \) M\( \Omega \), \( R_{jm} \gg 100 \) M\( \Omega \), and \( R_m \sim 100 \) M\( \Omega \)).

Equations (1) and (2) show that a reduction of \( R_{jm} \) or an increase in \( R_s \) improves the recording amplitude and the ability to manipulate \( V_m \) for stimulation. Case in point is that the membrane permeabilization (intracellular access) induced by the aforementioned injection of \( I_s \) reduces \( R_{jm} \) to decrease the attenuation of (1) by one to two orders: APs are measured from rat neurons with \( V_e \) of 1–30 mV [31], contrasting MEA
extracellular recording of APs in the range of 10–100 μV. Overall, the pCC allows intracellular recording of membrane potentials of a neuron with a current injection, where the current injection can be also used for concurrent stimulation. Finally, note only a small fraction (∼1%–10%) of $I_e \sim -1$ nA enters the permeabilized neuron, as $R_s \ll R_{jm} + R_m$.

Recently, a CMOS MEA [6] as well as our previous version of the CMOS nanoelectrode array [25] intracellularly recorded the membrane potential of cardiomyocytes without using the pCC but by applying a voltage to an electrode followed by a voltage recording. This voltage application also produces an electrode current to permeabilize the cell membrane for intracellular access. However, since the voltage application and voltage recording cannot be simultaneous, the electrode current is absent during the recording, and hence, the permeabilization-induced leakage from the cell cannot be compensated during the recording. This still did not prevent the intracellular recording of the membrane potentials of cardiomyocytes, as the tissue of the cardiac cells is electrically more robust due to their gap junction connections. However, this voltage-application voltage-recording approach deficient in leakage compensation cannot achieve stable intracellular recording of neuronal membrane potentials, as neurons are electrically isolated via chemical synapses and are, therefore, far more adversely affected by the leakage and the resulting depolarization.

### B. Pseudo-Voltage-Clamp Configuration

The pseudo-voltage-clamp (pVC) mode [see Fig. 4(b)] is obtained by disconnecting the current injector and configuring the feedback loop of the op-amp to form a transimpedance amplifier. The feedback resistance of the transimpedance amplifier is a switched capacitor, which utilizes the switches in parallel to the feedback dps and the parasitic capacitance $C_{par} \sim 35\, \text{fF}$ of the intermediate node between the sets of 2 and 4 dps [see Fig. 3(a)]. These switches are controlled in real time using the memory with non-overlapping clock phases $Φ_1$ and $Φ_2$. We set the effective resistance $R_{TIA} = 1/f_{TIA} C_{par}$ of the switched capacitor typically around ∼700 MΩ using a switching frequency $f_{TIA}$ of ∼40 kHz. The high-frequency pole of the transimpedance amplifier is set by the feedback capacitance $C_2$ in parallel with $R_{TIA}$.

In contrast to the commonly used integrate and reset scheme, which offers the lowest noise option for current measurement [35], the feedback switched capacitor allows for sampling of all pixels via the multiplexer regardless of their sampling position as the output voltage is never completely reset. Rather, a packet of feedback charge $ΔQ_{fb} = V_{amp} C_{par}$ is switched from the output to the negative terminal of the amplifier to “soft-reset” the voltage across $C_2$, which reaches a steady state across a switching period $1/f_{TIA}$ when it is equal to the transimpedance amplifier input current $I_{in} = ΔQ_{fb}/f_{TIA}$. The noise of this configuration is comparable to the integrate and reset scheme, as the input current is integrated across $C_2$ [35], except that we observe significantly more noise from pixels sampled during $Φ_1$ due to additional leakage current from 3 dps in parallel to the used switch [see Fig. 3(a)] (see Section V-C).

The pVC mode utilizes the transimpedance amplifier in applying a voltage $V_{s,1} = V_e$ to the electrode and simultaneously measuring the electrode current $I_e$. The bias point of $V_e$ is adjusted to set the bias value of $I_e$ at −1 nA, which induces membrane permeabilization for intracellular access. Then, the modulation of $V_e$ is used as a voltage stimulation to induce a change of the membrane potential $V_m$

$$\frac{ΔV_m}{ΔV_e} = \frac{R_m}{R_{jm} + R_m} \quad (3)$$

where we have used $|Z_e| \ll R_e, R_{jm}$, and $R_m$ and $R_s \ll R_{jm} + R_m$. The resulting membrane current (ion channel current, such as Na$^+$ spikes) $ΔI_m$ modulates the electrode current in the range of ∼100 pA–1 nA [31] according to

$$ΔI_m = \frac{R_m R_s}{R_e Z_e + R_{jm}(R_e + Z_e) + R_m(R_s + Z_e)} \approx \frac{R_m}{R_{jm} + R_m}. \quad (4)$$

This $ΔI_e$ is measured by the transimpedance amplifier. $ΔI_m$ is an attenuated version of $ΔI_m$ and contrasts the patch clamp’s voltage clamp that has no such front-end attenuation (and hence the prefix “pseudo” for our voltage clamp). However, the attenuation factor is greatly reduced due to the reduction of $R_m$ with the intracellular access (membrane permeabilization with the injection of the bias value of $I_e$), just like in the pCC case. On the other hand, unlike the pCC, increasing $R_e$ does not improve either the ability to
record or stimulate to the first order: as a small-signal model.

The corresponding small-signal output impedance, $Z_{OUT} = \frac{|V_{OUT}|}{I_{OUT}}$, is $R_{eff} = \frac{1}{f_{SC}C_{SC}}$.

To increase $Z_{OUT}$ substantially, we can build a source follower circuit around the switched capacitor, as shown in Fig. 5(b), to set $V_1 - V_{OUT}$ at a fixed value: the $V_1$ and $V_{OUT}$ nodes of the switched capacitor are connected to the source and gate of the PMOS transistor. $V_1$ then follows $V_{OUT}$ to maintain $V_1 - V_{OUT}$ at $V_{SG}$, i.e., the source–gate voltage of the transistor. In the absence of channel length modulation, $V_{SG}$ is fixed at a constant value by the bias current $I_0$ and independent of $V_{OUT}$. In this ideal case, $\frac{T_{OUT}}{f_{SC}C_{SC}}(V_1 - V_{OUT}) = f_{SC}C_{SC}V_{SG}$ is perfectly independent of $V_{OUT}$ and can be set by $f_{SC}$ and $C_{SC}$ to a constant value. Correspondingly, $Z_{OUT} = \infty$. In the realistic case with the transistor channel length modulation, $V_{SG}$ does vary with $V_{OUT}$ but only weakly, so $\frac{T_{OUT}}{f_{SC}C_{SC}}(V_1 - V_{OUT}) = f_{SC}C_{SC}V_{SG}$ exhibits only a small dependence on $V_{OUT}$. The corresponding $Z_{OUT}$ calculated with the small-signal model of Fig. 5(c) is

$$Z_{OUT} = \frac{r_n}{(1 + g_m r_n)} = \frac{r_n}{(1 + g_m r_n)}$$

where $r_n$ is the output resistance of the PMOS transistor and the current ($I_0$) bias circuit, respectively, and $g_m$ is the transconductance of the PMOS transistor. The second line is approximated by setting $r_n \approx g_m r_n \approx r_n$ without losing the essence and by using $g_m r_n / 2 \approx 1$. As seen, $Z_{OUT}$ is greatly boosted from $R_{eff} = 1/f_{SC}C_{SC}$ by a factor of $g_m r_n / 2$.

**B. Transient Dynamics**

We now discuss the transient behavior of the switched-capacitor current injector of Fig. 5(b). During a clock phase $\Phi_1$, $C_{SC}$ is disconnected from $V_{OUT}$ and connected to $V_1$ via the switch on-resistance $R_{SW}$ ($R_{SW} \ll R_L$). Throughout this $\Phi_1$ phase, $V_{OUT}$ decays with a slow time constant of the load, $t_L = R_L C_L$, and $V_1$ follows this decay to maintain $V_1 = V_{OUT} + V_{SG}$ [see Fig. 6(a)]. In contrast, at the onset of the phase $\Phi_1$, the switched-capacitor voltage $V_{SC}$ makes a rapid upward transition from $V_{OUT}$ to $V_1 = V_{OUT} + V_{SG}$ [see Fig. 6(a)]. Rapidly charging $C_{SC}$ (time constant: $t_1 = R_{SW}C_{SC} < 1 \text{ ns} \ll t_L$) with $\Delta Q_{SC} = C_{SC} \Delta V_{SC} = C_{SC}V_{SG}$.

During the subsequent clock phase $\Phi_2$, $C_{SC}$ is disconnected from $V_1$ and connected to $V_{OUT}$ via $R_{SW}$.

This reconfiguration rapidly redistributes the charge $\Delta Q_{SC} = C_{SC}V_{SG}$ between $C_{SC}$ and $C_L$ with a fast time constant $t_2 = R_{SW}C_L C_{SC}/(C_L + C_{SC}) \approx R_{SW}C_L < 1 \text{ ns} < t_L$, discharging $C_{SC}$ (lowering $V_{SG}$) and charging $C_L$ (raising $V_{OUT}$) until $V_{SC} = V_{OUT}$ [see Fig. 6(a)]. The resulting change of the output voltage $\Delta V_{OUT}$ is

$$\Delta V_{OUT} = \frac{\Delta Q_{SC}}{C_{SC} + C_L} = \frac{C_{SC}V_{SG}}{C_{SC} + C_L} \approx \frac{C_{SC}V_{SG}}{C_L}$$

These changes of $V_{SC}$ and $V_{OUT}$ ($V_1$ follows $V_{OUT}$ to maintain the difference $V_{SG}$) occur rapidly during the very early part of the phase $\Phi_2$ due to the short time constant $t_2$ [see Fig. 6(a)]. The charge packet injected to $C_L$ during the charge redistribution in the early part of $\Phi_2$ is $\Delta Q_{OUT} = C_L\Delta V_{OUT}$.
The output current $I_{OUT}$ is due to this charge packet injection, and its average over a clock period is given by

$$I_{OUT} = f_{SC} \Delta Q_{OUT} = f_{SC}C_{SC}V_{SG} \times \left[ \frac{C_L}{C_{SC} + C_L} \right]$$

which is consistent with the calculation of Section IV-A.

With repeated clock cycles, $V_{OUT}$ is then a sequence of a rapid $\Delta V_{OUT}$ up-step (time constant $\tau_2$) followed by a slow decay (time constant $\tau_L$) [see Fig. 6(a)]. If we break down $I_{OUT}$ into current $I_{OUT,R}$ through $R_L$ and current $I_{OUT,C}$ through $C_L$ ($I_{OUT} = I_{OUT,R} + I_{OUT,C}$) in phase $\Phi_2$, the rapid charging of $C_L$ in the beginning of $\Phi_2$ is described by $I_{OUT} \approx I_{OUT,C} > 0$, while the background slow discharging of $C_L$ through $R_L$ is described by $-I_{OUT,R} \approx I_{OUT,R} (I_{OUT,R} < 0)$ with $I_{OUT} \approx 0$ [see Fig. 6(a)]. In the initial clock cycles, the charging of $C_L$ by the charge packet injection $\Delta Q_{OUT} = C_L \Delta V_{OUT}$ per clock cycle exceeds its discharging through $R_L$ per clock cycle, and thus, $V_{OUT}$ overall rises, but once $C_L$ is sufficiently charged at later clock cycles, its charging state, ignoring the ripples, can be quantified by evaluating $V_{OUT}$ at $t = n/f_{SC}$ or at the end of $n$th clock phase $\Phi_2$ as follows:

$$V_{OUT}(t) = \Delta V_{OUT} \sum_{k=1}^{n} \exp \left( -\frac{k}{f_{SC}R_LC_L} \right) \times \exp \left( -\frac{1}{2f_{SC}R_LC_L} \right) \approx \frac{\Delta V_{OUT}}{R_L} \left[ 1 - \exp \left( -\frac{t}{R_LC_L} \right) \right]$$

where we have used $f_{SC}R_LC_L > 1$ and (6) and (7). This converges to $\frac{\Delta V_{OUT}}{R_L}$ in steady state [see Fig. 6(b)], i.e., in the steady state, $I_{OUT}$ flows into the electrode to charge $C_L$, and then, exactly the same amount of charge leaks out through $R_L$ as expected. This is equivalent to flowing $\frac{\Delta V_{OUT}}{R_L}$ through $R_L$. In fact, the overall voltage response of the $R_LC_L$ load to the switched-capacitor current injector captured by (8), ignoring the ripples [$\Delta V_{OUT}$ of (6)], is identical to the voltage response of the $R_LC_L$ load to an ideal step current with a magnitude $\frac{\Delta V_{OUT}}{R_L}$ [see Fig. 6(b)]. This justifies our current injector as a constant current injector. The foregoing discussion has assumed $\frac{\Delta V_{OUT}}{R_L} < V_{DD} - V_{OV} - V_{SG}$ ($V_{OV}$: overdrive voltage of the current mirror transistor); if $\frac{\Delta V_{OUT}}{R_L} > V_{DD} - V_{OV} - V_{SG}$, $V_{OUT}$ will start to roll off and be clipped at $V_{DD}$ [see Fig. 6(b)].

In the pCC mode, the current injector is connected to the electrode (so $V_e = V_{OUT}$ and $I_e = I_{OUT}$) and runs in parallel with the voltage amplifier [see Fig. 4(a)], where $\Delta V_{OUT} = 0.1 \sim 50$ mV for $C_L = 1 \sim 100$ pF. This ripple voltage could interfere with the recording of $\Delta V_e = 1 \sim 30$ mV. We minimize this interference using clock synchronization (see Section IV-D).

### C. Implementation

The actual switched-capacitor-based current injector that we implement is shown in Fig. 7(a). It can inject both positive and negative currents. The polarity is controlled by turning on either current source $I_{0,p}$ or $I_{0,n}$ to reduce the circuit to either Fig. 7(b) for positive injection, $I_{OUT} \approx f_{SC}C_{SC}V_{SG,PMOS} > 0$, or Fig. 7(c) for negative injection, $I_{OUT} \approx -f_{SC}C_{SC}V_{SG,NMOS} < 0$. For pCC recording, we use the NMOS configuration of Fig. 7(c) to set $I_e \sim -1$ nA, as negative current enables intracellular access [see Fig. 4(a)]. Here, we do not balance the negative injection with a positive injection for a given clock frequency in order to minimize the amount of circuitry and corresponding area: it is only used as a negative current injector for the intracellular experiments.

The bottom of Fig. 7(d) (solid red box) shows the transistor-level schematic of Fig. 7(a). The core switched-capacitor circuit uses two transmission gates and can add 10 or 100 fF to the parasitic capacitance $C_{SC,p} \sim 30$ fF of the $V_{SC}$ node for $C_{SC}$. We remove the body effect of transistors $M_b$ and $M_p$ to minimize the $|V_{SG}|$ dependence on $V_{OUT}$ by tying the source and body nodes in both the PMOS and NMOS transistors (the 0.18-μm technology that we use is a triple-well process). A control signal $EN_{POS}$ in the bias network enables either the $I_{0,p}$ or $I_{0,n}$ current sources of Fig. 7(a) for positive or negative injection. The clock can be selected from three clock inputs $CLK[1:3]$, and this enables flexible control of $f_{SC}$ across the 4096 pixels.

### D. Clock-Sampling Synchronization

As the current injector in the pCC configuration utilizes switched capacitances, $f_{SC}$ is synchronized to the pixel multiplexer to minimize aliasing of switching induced noise, $\Delta V_{OUT}$ of (6), in the recorded amplifier output signal, $V_{amp}$. The aliased $\Delta V_{OUT}$ amplitude dominates the noise of the...
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Fig. 7. (a) Current injector that we implement. (b) With $I_{0,p}$ ON and $I_{0,n}$ OFF, (a) is reduced to what is shown here, capable of positive current injection. (c) With $I_{0,n}$ ON and $I_{0,p}$ OFF, (a) is reduced to what is shown here, capable of negative current injection. (d) Transistor-level schematic of the current injector, including the non-overlapping clock generation circuit. Control signals CLK[1:3], ENSC, ENSP, ENC1, and ENC2 are controlled by the pixel’s transparent latch memory.

pCC configuration and is larger than any parasitic charge injection or clock feedthrough as it is directly related to the discharging of the switched capacitor into the current injector’s output node/input of the amplifier. To start, $V_{amp}$ is sampled by a 128:1 output multiplexer [see Fig. 3(a) and (c)] operated at a frequency of $f_s \sim 1.2$ MHz resulting in a pixel sample frequency $f_{s,pixel} = f_s/128 \sim 9.4$ kHz. To synchronize $f_{SC}$ to $f_{s,pixel}$ across all 128 pixels in the multiplexer, $f_{SC}$ should be an integer multiple of $f_{s,pixel}$ ($f_{SC} = nf_{s,pixel}$, $n = 1, 2, \ldots$), while $f_s$ should be an integer multiple of $f_{SC}$ ($f_s = mf_{SC} = 128f_{s,pixel}$, $m = 1, 2, \ldots$). Taken together ($n \cdot m = 128$), $f_{SC}$ must be a power of 2 multiple of $f_{s,pixel}$ to eliminate aliasing ($f_{SC} = 2^N f_{s,pixel}$, $N = 0, 1, 2, \ldots$).

However, this constraint limits the resolution of injected current as $I_{out} \propto f_{SC}$. To elaborate, the minimum $I_{OUT}$ at $f_{s,pixel} \sim 9.4$ kHz would result in available $I_{OUT}$ of only 150 pA, 300 pA, 600 pA, 1.2 nA, 2.4 nA, and so on. To obtain a higher resolution in the injected current, a nonsymmetric clocking scheme is used for the generation of $f_{SC}$ (see Fig. 8). Effective single integer multiples are established by spacing $n$ pulses as evenly as possible with $1/f_s$ resolution throughout the total multiplexer period of $1/f_{s,pixel} = 128/f_s$ [see Fig. 8(a)]. The resultant digital bitstream is then repeated at $128/f_s$ (equivalent to $1/f_{s,pixel}$, ~100 μs) to form a continuous output. The current resolution used for experiments is then $n \cdot 150$ pA, $n = 1, 2, \ldots, 64$. The non-symmetrical switching can increase $\Delta V_{OUT}$ by up to 50% at $n = 63$ [see Fig. 8(b)], yet the synchronization minimizes this increase from affecting the signal measurement. A dedicated microprocessor is used to generate the nonsymmetric clocks (CLK[1:3] in Fig. 7). During experiments (see Section VI-A), we observe low-frequency $\Delta V_{OUT}$ noise most likely due to clock drift between the microprocessor and acquisition electronics.

The same synchronization scheme is used for the pVC configuration, whose transimpedance amplifier also uses a switched capacitance. In this case, we commonly set $f_{TIA} = 4f_{s,pixel} = 37.6$ kHz to minimize switching noise.

V. ELECTRICAL CHARACTERIZATION

A. Experimental Setup

The IC is packaged and placed on a printed circuit board (PCB) (see Fig. 9). The IC and PCB are programmed and read through three National Instruments PXIe-6358 data acquisition (DAQ) cards and interfaced to a computer through
Fig. 9. System architecture of the IC and external electronics showing analog and digital signal flow.

LabVIEW software. For digital programming, each pixel is addressed in a shift register (4096 bits) with real-time adjustment/latching of the bit lines (B[1:25] in Fig. 3). For recording, the 4096 pixel amplifier outputs are divided into 32 subgroups. Each subgroup contains 128 outputs from two rows of the array, feeding its own 128:1 analog output multiplexer on chip. Each of the 32× distributed in-pixel multiplexers, as shown in Fig. 3(c), right, consumes 0.45 mW of total power; 32 NMOS source followers, each consuming 6.86 mW, are then used to buffer the 32×128:1 multiplexer outputs from the IC to 32×16 bit ADCs of the DAQ cards. Adjacent pixel-to-pixel crosstalk within the multiplexer was measured at −43 dB. The overall data rate of recording is 77 MB/s.

The IC’s $V_{SS}$ is set to earth ground and $V_{DD} = 3.6$ V; this is set higher than the 3.3-V transistors that we use, in order to increase both output and stimulation voltage ranges. The $V_{s1}$–$V_{s4}$ nodes are connected to DAQ analog outputs that are low-pass filtered ($f_{-3dB} \approx 1$ Hz) to provide bias voltages or buffered with a bandwidth of $\sim 100$ kHz to provide voltage signals for various pixel circuit characterizations. The extracellular solution is biased using a Pt or Ag/AgCl reference electrode at $V_{ref}$, which is adjustable from 0 to 3.6 V. To regulate the temperature for cell health, the two temperature sensor signals from the IC are fed to an analog PI controller on the PCB, which then sets the voltage of a regulator on the PCB to drive the integrated heater. The designed accuracy for the temperature regulation is $<1$ °C and is calibrated using a thermocouple placed on the surface of the device in solution. In addition to the IC’s total power dissipation of 1.25 W when the array is fully enabled, the heater typically dissipates 0.55–0.85 W to maintain 35 °C (see Table I). This extra power dissipation is needed to overcome heat loss of the solution on top of the device to the ambient environment and contrasts with MEAs designed for interfacing to thermally insulating tissues or environments. Like the integrated pixel array, the PCB is designed to be highly configurable to ensure ample experimental flexibility and is adjusted using analog switches digitally controlled through a serial interface.

Table I

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<td>Current injector (x4096)</td>
<td>24 μW</td>
</tr>
<tr>
<td>Output multiplexer (x32)</td>
<td>7.3 mW</td>
</tr>
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<td>Fully enabled array power consumption</td>
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<tr>
<td>Maximum heater power</td>
<td>1.3 W</td>
</tr>
<tr>
<td>Typical heater power to maintain 35°C</td>
<td>0.55 – 0.85 W</td>
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</table>

![Fig. 10. (a) Positive and negative $I_{OUT}$ versus $f_{SC}$ for $V_{OUT} = 1.8$ V. (b) Positive and negative $I_{OUT}$ versus $V_{OUT}$ for $f_{SC} = 100$ kHz.](image)

B. Measurement of Pixel Current Injector

We first characterize the pixel current injector by connecting $V_{OUT}$ to the PCB via $V_{s3}$, bypassing the pixel electrode and the solution. Fig. 10(a) shows the measured positive and
negative $\Delta I_{\text{OUT}}$ versus $f_{\text{SC}}$ (1 kHz to 10 MHz) for $V_{\text{OUT}} = V_{i,3} = 1.8$ V ($V_{\text{DD}} = 3.6$ V and $V_{\text{SS}} = 0$ V). They confirm the linear response of $\Delta I_{\text{OUT}}$ to $f_{\text{SC}}$ over the four decades of frequency, from which we extract $V_{\text{GSPMOS}} = 0.63$ V, $V_{\text{GSNMOS}} = 0.56$ V, and $C_{\text{SC,p}} = 26$ fF. The minimum $|I_{\text{OUT}}|$ is $\approx 15$ pA at $f_{\text{SC}} = 1$ kHz, and the maximum $|I_{\text{OUT}}|$ is $\approx 0.7$ μA at $f_{\text{SC}} = 10$ MHz. To demonstrate the weak dependence of $\Delta I_{\text{OUT}}$ on $V_{\text{OUT}}$, $V_{\text{OUT}} = V_{i,3}$ is swept from 0 to 3.6 V while fixing $f_{\text{SC}}$ at 100 kHz. Both currents show flat responses [see Fig. 10(b)], with the positive $\Delta I_{\text{OUT}}$ rolling off around $V_{\text{DD}} - V_{\text{GSPMOS}} \approx 3.0$ V and the negative $\Delta I_{\text{OUT}}$ rolling off around $V_{\text{SS}} + V_{\text{GSNMOS}} \approx 0.6$ V. The measured variations of $|I_{\text{OUT}}|$ in the flat regions are only within $\approx 5\%$ for $C_{\text{SC}} = C_{\text{SC,p}}$. Its deviation from theoretical 0.3% is due mainly to the voltage dependence of $C_{\text{SC,p}}$ (for $C_{\text{SC}} = 100$ fF + $C_{\text{SC,p}}$ where the $C_{\text{SC,p}}$ effect is weaker, the current variation is reduced to $< 2\%$). In addition, this variation of $\Delta I_{\text{OUT}}$ is approximately inversely proportional to $f_{\text{SC}}$ [see (5)]. The discrete negative injection levels for the clocksampling synchronization scheme (see Section IV-D) were then measured using $C_{\text{SC}} = C_{\text{SC,p}}$, i.e., the configuration used for the pCC intracellular measurements. For the pixel shown in Fig. 11, left, $I_{\text{OUT}}$ is at distinct multiples of $-147$ pA, corresponding to $n f_s$, pixel. At $n = 8$, $I_{\text{OUT}}$ shows $< 5\%$ variation around $\approx 1.2$ nA across the array. To measure the output ripple voltage $\Delta V_{\text{OUT}}$ [see (6)] and to highlight the ability for small amplitude current injection, the current injector was tested in a solution using a small, 2-μm-diameter Pt electrode (with no PtB deposition) post-fabricated on the pixel pad. This post-fabrication involves photolithography to define the hole, dry etching of the foundry passivation to expose the Al pad, deposition of 20-nm Ti and 200-nm Pt, and liftoff [31]. The pixel op-amp was configured as a buffer to measure the voltage ripple during the current injection. We increase $f_{\text{SC}}$ from 0 Hz to 1 kHz and then decrease it back to 0 Hz, all in 200-Hz increments (see Fig. 12, bottom). This results in $\approx 5$-pA step current increases/decreases for positive/negative injections (see Fig. 12, top). The ripple voltage can be clearly seen (see Fig. 12, middle, at $f_{\text{SC}} = 600$ Hz), with $\approx 20$-mV step size for both positive and negative injections. This ripple voltage for the 2-μm-diameter Pt electrode with $C_L = 1.7$ pF being much larger (est. $50 \times$) than the ripple voltage for the PtB electrode that has a much larger $C_L$ due to its rough surface texture that increases its surface area. These time-dependent behaviors of $\Delta I_{\text{OUT}}$ and $V_{\text{OUT}}$ are consistent with the theoretical considerations of Section IV-B (see Fig. 6). C. Measurement of pCC and pVC Amplifiers

The pCC amplifier configuration was first tested to investigate the optimal number of feedback dps for voltage amplification: the input ($V_{i,1}$) and output ($V_{\text{amp}}$) dc transfer curve was measured for each of the 0–7 dps options across the array [see Fig. 13(a)]. This test is important to ensure array-wide operation: leakage currents across the multiple feedback dps can induce offset voltages that can saturate the amplifier, reducing the number of available pixels. Sharp transitions of
the array wide median $V_{\text{amp,dc}}$ from the lower (0.2 V) to upper (2.8 V) output voltage rails for increasing the number of feedback dps show their sensitivity to the leakage currents (see Fig. 13(a), right). To overcome this sensitivity, not only do we choose the optimal number of feedback dps but we also use the dp connected to $V_{\text{dc}}$ to set a current across the feedback dps to tune their offset and impedance.

For the extracellular recording of the membrane potential (this is done later in Section VI by setting $I_p = 0$ in the pCC configuration so as not to cause membrane permeabilization), we use two feedback dps in parallel to $C_2 = 5 \text{ fF}$ to set a passband gain of 275 V/V with a bandwidth $f_1 = 100 \text{ Hz}$ to $f_2 = 5 \text{ kHz}$ [see Fig. 13(b)]. The 100-Hz pole substantially filters out the $1/f$ noise, given that the open-loop amplifier has a $1/f$ noise corner of $\sim 10 \text{ Hz}$. The measured input-referred noise is $5.6 \mu V_{\text{rms}}$ when integrated from 1 Hz to 4.7 kHz [see Fig. 13(b)].

The pCC intracellular recording mode (done later in Section VI with non-zero $I_p$) must deal with larger amplitude signals ($\Delta V_e > 1 \text{ mV}$ or $\Delta V_{\text{amp}} > 300 \text{ mV}$). In this case, since the two feedback dps exhibit non-linear clipping, we instead use six feedback dps to lessen the voltage seen on each dp with large output voltages. In this configuration, the feedback current is especially essential to control $V_{\text{amp,dc}}$ across the array that would otherwise be saturated due to the sharp slope observed in Fig. 13(a) with 6 dps. With this measure, signals as large as $\Delta V_e > 20 \text{ mV}$ can be recorded without distortion.

On the other hand, the large impedance of the 6 dps causes $f_1 < 1 \text{ Hz}$; this lets in a larger amount of $1/f$ noise (as the open-loop amplifier has the $1/f$ corner at $\sim 10 \text{ Hz}$), resulting in an increased integrated input-referred noise of $\sim 23 \mu V_{\text{rms}}$ at $A_0 = 30 \text{ V/V}$ [see Fig. 13(b)]. Digital filters can reduce this additional low-frequency noise depending upon the signal frequencies of interest (e.g., PSPs range from $\sim 100 \text{ Hz}$ to 1 kHz).

Fig. 14 shows the characterization of the pVC transimpedance amplifier. Input current $I_{\text{in}}$ is applied using $V_{\text{dc}}$ through $C_1 = 3.5 \text{ pF}$ (see Fig. 14(a), left) to measure the transimpedance gain $R_{\text{TIA}} \sim 700 \text{ M}\Omega$ for $f_{SC,pVC} = 4f_{\text{pixel}} = 37.6 \text{ kHz}$ and for $V_{r,1} = 1.0 \sim 2.4 \text{ V}$ (see Fig. 14(a), right). The bandwidth of the transimpedance amplifier extends from dc to 2-kHz set by $R_{\text{TIA}}$ and $C_2 = 100 \text{ fF}$ (see Fig. 14(b), left) with an input-referred noise as low as $1.1-pA_{\text{rms}}$ integrated from 1 Hz to 4.7 kHz (see Fig. 14(b), right). Gain and noise measurements across the array show a distinct spatial dependence due to multiplexer sampling and its relation to the clock phases [see Fig. 14(c)]: pixels that are sampled during $\Phi_1$ exhibit larger noise and gain in comparison to $\Phi_2$. These variations could be optimized in future designs by incorporating a dedicated switched feedback element synched to the multiplexer in the pixel circuit and using a traditional integrator and reset method for the lowest noise performance [35].

![Diagram](image1)

**D. Characterization of Electrode and Routing Capacitance**

For optimal pCC and pVC coupling [see (1)–(4)], we desire a small electrode impedance ($Z_e$) or a large electrode capacitance $C_e$. Concretely, $C_e \gg (C_p, + C_1)$ is the condition to obtain the final expression in (1), eliminating the attenuation due to the electrode; $|Z_e| \ll R_s, R_{\text{jm}}$, is the condition to obtain the final expressions of (3) and (4) with no attenuation due to the electrode. To minimize $Z_e$ (i.e., to increase $C_e$), PtB is electrodeposited onto Pt electrodes post-fabricated on the Al pads, as the surface roughness of PtB increases the electrode surface area (e.g., Fig. 15, right) [31]. For the PtB deposition, $V_{r,1}$ is used to apply a voltage ramp to $V_e$ from 0 to $\sim 1.2 \text{ V}$ at 50 mV/s with respect to a Pt reference in a solution of 0.5-mM H$_2$PtCl$_6$ and 25-mM NaNO$_3$ [36]. $Z_e$ is measured across the array periodically throughout the deposition by applying a 1–25-mV, 5-kHz sine wave sequentially to each pixel and measuring the resultant current through the

![Diagram](image2)

![Before PtB](image3)

![After PtB](image4)

![SEM images](image5)
Fig. 17. Example of the extracellular recording of a dissociated rat neuron using a PtB planar hole electrode.

VI. ELECTROPHYSIOLOGICAL MEASUREMENTS

We demonstrate pCC and pVC intracellular recording and stimulation with dissociated rat neurons, cultured on the IC for 10–14 days in vitro. We use PtB vertical nanoneedles for pVC and PtB vertical nanoneedles with pad edge electrodes for pCC [31]. Fig. 17 shows an example extracellular signals recorded using the high-gain, low-noise voltage amplifier configuration of our CMOS IC—similar to other CMOS MEAs [1]–[14]—as a reference for comparison to the intracellularly recorded signals that we will present now.

A. pCC Neuron Measurements

To demonstrate the pCC operation, we first determined the threshold $I_e$ needed for intracellular access by changing $I_e$ from $0 \sim -3.0$ nA with a step of $-150$ pA and measuring $V_e$ with the rat neurons on top [see Fig. 18(a)]. The threshold $I_e$ was determined when $V_e$ substantially increased, and APs were clearly distinguished [see Fig. 18(a)]. The intracellular threshold so determined lied between $-1.1$ to $-2.2$ nA across the array.

To quantify the overall noise at the electrode beyond the input-referred noise of the pCC amplifier, we performed two types of experiments. First, we measured $V_e$ for various bandwidths again by changing $I_e$ from $0 \sim -3.0$ nA, but this time without a neuron above (Fig. 18(b), left) shows the data for an
TABLE II
Performance Comparison of State-of-the-Art CMOS Microelectrode and Nanoelectrode Arrays

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<th>[3]</th>
<th>[4], [14]</th>
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<th>[6]</th>
<th>[25] (Our prior work)</th>
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<td>0.18 μm</td>
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<td>0.13 μm</td>
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<td>Planar microelectrode</td>
<td>Planar microelectrode</td>
<td>Planar microelectrode</td>
<td>Vertical nanoelectrode</td>
<td>Vertical nanoelectrode with surface roughness</td>
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<td>- / ±32 μA</td>
<td>±1.65 V / ±382.5 nA</td>
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<td>±5 pA (140 pA for pCC)</td>
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example pixel). Second, we measured $V_r$ with the $L$ below the intracellular threshold so that no intracellular coupling occurs even if there is a neuron above (Fig. 18(b), right shows the data across the array). These experiments show that on top of the $\sim 23\mu V_{rms}$ input-referred noise of the pCC intracellular-mode amplifier (see Section V-C), there is an additional noise
PSPs (EPSPs) are clearly measured with threshold sensitivity is shown in Fig. 18(c), where excitatory signal measurement is also possible. An example of such subthreshold sensitivity of more than 1700 neurons in parallel for a recording was demonstrated with an intracellular measurement of 304 synapses between 396 neurons, which demonstrates cross-pixel AP to PSP correlation that allowed mapping lar coupling rate [31]. The subthreshold sensitivity enabled to measure $I_e$ and adjust $V_e$ simultaneously, allowing for the concurrent intracellular recording of ion channel currents and stimulation of membrane potentials.

Such intracellular ion-channel measurement of mammalian neurons can be useful for high-throughput drug screening applications, where current high-throughput intracellular tools, i.e., the planar patch clamp, are limited to non-neuronal, artificial cell lines. As a first demonstration toward this end, we measured the effects of ion-channel drugs affecting both the Na$^+$ and K$^+$ currents of the dissociated rat neurons [31].

B. pVC Neuron Measurements

To demonstrate the pVC operation, we gradually increased the magnitude of $V_e$ to determine the threshold for intracellular access (see Fig. 19). Since no spontaneous activity is observed for pVC due to its low input impedance, voltage stimulations were applied to activate the neuron’s ion channels: at $V_e = -0.65$ to $-0.7$ V, distinct Na$^+$ spikes and K$^+$ repolarization currents are observed during stimulation, clearly distinguished in the high-pass (100-Hz) filtered version of the measured electrode current $ΔI_e$. The pVC mode clearly enables the ability to measure $I_e$ and adjust $V_e$ simultaneously, allowing for the concurrent intracellular recording of ion channel currents and stimulation of membrane potentials.

Fig. 19. Ramped $V_e$ experiments in the pVC configuration to determine the threshold for intracellular access using a PtB nanoneedle electrode and dissociated rat neurons. $V_e$ stimulations are applied to activate ion channels.

of $40 \sim 150 \ \mu V_{\text{rms}}$ largely below 10 Hz in frequency. This extra noise originates from the electrode ($\sim10 \ \mu V_{\text{rms}}$), solution ($\sim30 \ \mu V_{\text{rms}}$ [12]), and the current injector’s ripple voltage ($0 \sim 110 \ \mu V_{\text{rms}}$, dependent upon $|I_e|$). If the clock of the switched-capacitor current injector and that of the output multiplexer were perfectly synchronized, the ripple voltage noise would disappear in its entirety (see Section IV-D), but, in reality, the two clocks slightly drift from each other at low frequencies below 10 Hz, which aliases the ripple voltage into the recording noise at the low frequencies. The non-uniformity of the noise across the array (see Fig. 18(b), right) is attributed to variations in $f_1$ arising from feedback diode leakage current variation. By comparing this overall noise to the AP amplitudes of $1 \sim 30$ mV measured at the electrode in the pCC intracellular mode (e.g., Fig. 18(a), right), we obtain a signal-to-noise ratio $>20$, on par with the patch clamp. The signal-to-noise ratio for PSPs is also $>1$, so subthreshold (synaptic) signal measurement is also possible. An example of such subthreshold sensitivity is shown in Fig. 18(c), where excitatory PSPs (EPSPs) are clearly measured with $ΔV_e$ amplitudes of $\sim200 \ \mu V \sim 1$ mV at the electrode.

A stimulation experiment with intracellular coupling at $I_e \sim -1.1$ nA with periodic $+550$-pA injections [see Fig. 18(d)], during which increased neuron AP firings are observed, demonstrates the ability to intracellularly record $ΔV_e$ and adjust $I_e$ simultaneously to stimulate the neuron through the same electrode.

The scalability of the device for network-wide intracellular recording was demonstrated with an intracellular measurement of more than 1700 neurons in parallel for a $>40\%$ intracellular coupling rate [31]. The subthreshold sensitivity enabled cross-pixel AP to PSP correlation that allowed mapping of 304 synapses between 396 neurons, which demonstrates the capability of the IC for synaptic connectivity mapping applications [31].

VII. Conclusion

We have presented the CMOS IC that contains 4096 pCC/pVC pixel circuits, with each connected to a PtB electrode. The electrodes form a dense, 20-$\mu$m pitch 64 $\times$ 64 array. Overall, the IC enables large-scale intracellular recording of neurons with the ability of simultaneous excitations. It is the flexibility of the pixel circuit, containing a new switched-capacitor-based current injector and a highly configurable op-amp, that enables both the pCC and pVC modes within each pixel circuit. The lateral separation of the pixel circuit from the electrode decouples the electrode pitch from the larger pixel circuit area for the low-noise design with the high configurability. The device has been fabricated in 0.18-$\mu$m CMOS technology, electrically characterized, and verified biologically with $\textit{in vitro}$ rat neurons. We summarize and compare the performance of this CMOS nanoelectrode array to start-of-the-art CMOS MEAs as well as our prior CMOS nanoelectrode array in Table II [3]–[6], [14], [25].

References


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